

應用於行動電話之高效率多頻帶CMOS功率放大器

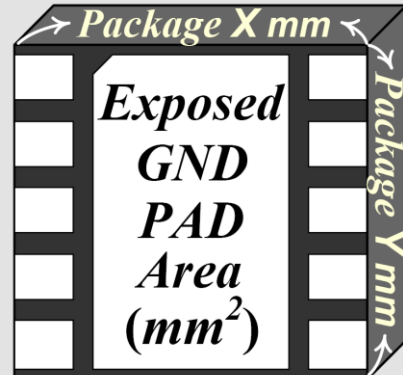
Highly-efficient Multi-band CMOS Power Amplifier for Mobile Phone Applications

4G in the Apple iPhone 5s & 5c

Support Standards	Support uplink bands (MHz)	Duplex Mode	Model: A1530 / A1529
LTE	B1: 1920-1980	FDD	√
	B2: 1850-1910	FDD	√
	B3: 1710-1785	FDD	√
	B4: 1710-1755	FDD	
	B5: 824-849	FDD	√
	B7: 2500-2570	FDD	√
	B8: 880-915	FDD	√
	B13: 777-787	FDD	
	B17: 704-716	FDD	
	B18: 815-830	FDD	
	B19: 830-845	FDD	
	B20: 832-862	FDD	√
	B25: 1850-1915	FDD	
	B26: 814-849	FDD	
	B38: 2570-2620	TDD	√
	B39: 1880-1920	TDD	√
	B40: 2300-2400	TDD	√

Evolution of GaAs PA Module

	Ref.	[8]	[9]
Size $\begin{matrix} X \\ Y \end{matrix}$		3 3	2 2.5
Exp. Area		4.2	1.5
Support LTE Bands		7	7 38 40 41



The diagram shows a 3D perspective of a rectangular package. The top face is labeled 'Exposed GND PAD Area (mm²)'. The top edge is labeled 'Package X mm' and the right edge is labeled 'Package Y mm'.

Challenge of the 4G LTE

Standard	Peak to Average Ratio	Channel BW
GSM	0 dB	200 KHz
EDGE	3.2 dB	200 KHz
CDMA2000	4.0 dB	1.25 MHz
WCDMA	3.5 dB	5 MHz
LTE	8.2 dB	20 MHz

Motivation of this Work

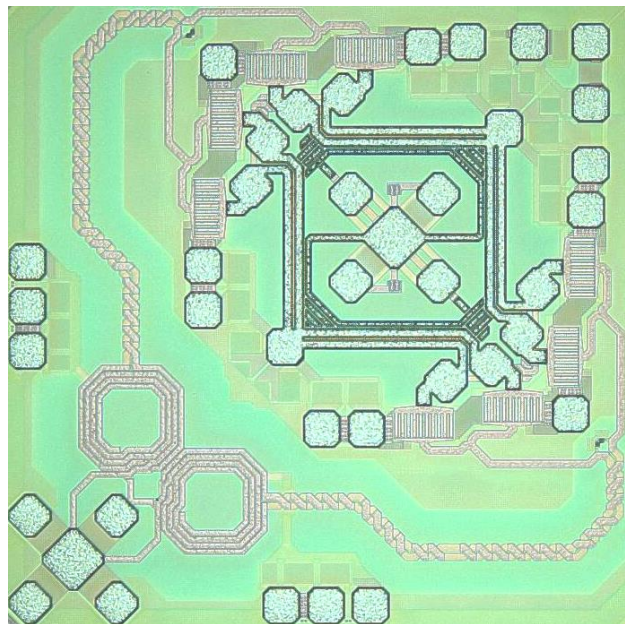
- Such support of LTE operating bands has been a major obstacle in lowering the cost and complexity of a mobile phone since the multiple PA modules must be used.
- ➔ Design a wideband PA to cover several LTE adjacent frequency bands for reducing the number of PA modules.
- PA modules have been known to consume most of the power and PCB area in the analog/RF front-end of a wireless communication device, and they also determine the talking and internet times.
- ➔ Considering benefits of integration and long-term development, it would be desired to have CMOS PAs evolve toward nanometer CMOS technologies and integrated into RF transceivers while keeping the chip size close to present day GaAs PAs also with high efficiency to mitigate the design issues in mobile phones.

Measured results of 90-nm Compact PA

Support LTE band-7, 38, 40, 41

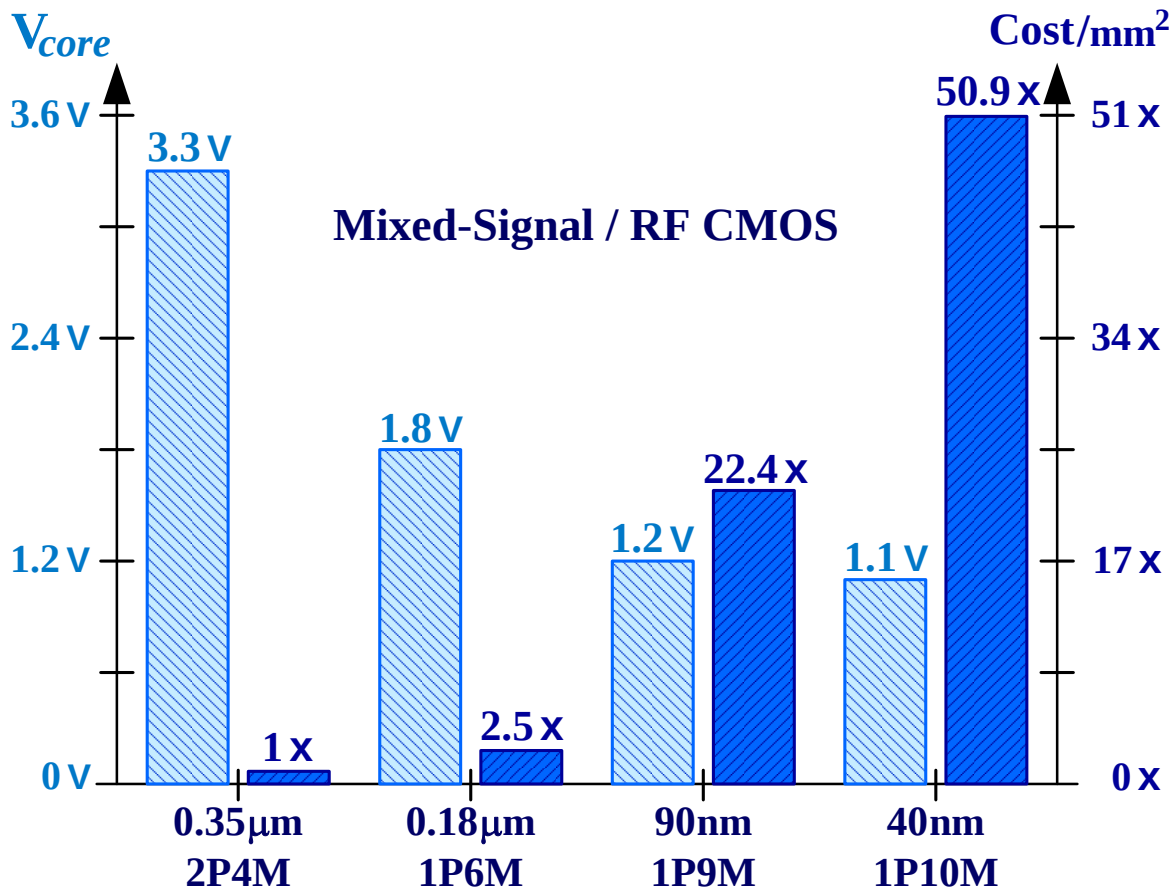
Freq.	Vdd	Max. Pout	Drain Eff.
2.4 GHz	1.2 V	27.3 dBm	47%
Class	Top metal	XFMR Eff.	Mp of CVT
AB	Cu 3.4 μm	79%	4 diff. CS
Equiv. Lp	1-dB BW	CMOS	Die size
0.9 nH	630 MHz	90 nm	0.99 mm ²

995 μm



995 μm

Scaling Trend of CMOS Technologies



Conclusion & Contribution

- ◆ Demonstrate the proposed **1:n concentric vortical transformer (CVT)** using **slab inductors** with the capability of efficiently and uniformly combining the power of several identical differential power cells.
- ◆ The CVT achieves the **less variation** of average input impedance and the much **less mismatch** of impedance among each input port as compared to the DAT with the same dimension.
- ◆ Demonstrate a **highly-efficient 90-nm fully-integrated CMOS linear PA** architecture using a **coupled L-shape CVT (CL-CVT)** and an **8-shape input balun** with the **negligible IR-drop impacts** while keeping all essential **bonding wires within a feasible length**.
- ◆ The proposed **low supply-voltage PA** is the **world's smallest** fully-integrated nanometer CMOS PA with the ability of saving about a half of chip area, **covering several adjacent LTE bands**, and passing the linear requirements without using any pre-distortion or calibration.